

J1050 U.S. PTO
10/078766
02/19/02

BEST AVAILABLE COPY

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10078766	02/19/2002	205		1741	Leader

**APPLICANTS: Miura Takeshi; Seita Masaru; Ota Yasuo;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB ☐ DO NOT PUBLISH

RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiners's initials

ATTORNEY DOCKET NO

51380

TITLE : Process for electroplating silicon wafers

U.S. DEPT. OF COMM./PAT. & TM.-PTO-435L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.				

FILED WITH:

☐ DISK (CRF)

☐ CD-ROM

(Attached in pocket on right inside flap)